Remarks:

Reconsideration of the application is requested. Claims 12-27 are now in the application. Claims 12-14 and 18 have been amended. Claim 11 has been canceled. Claims 22-27 have been added.

In item 4 of the Office action, the Examiner rejected claims 11-12 as being fully anticipated by Hirano et al. (U.S. 5,812,022) under 35 U.S.C. § 102(b). In addition, in item 6 of the of the Office action, the Examiner rejected claims 18-19, and 21 as being unpatentable over Hirano et al. in view of Olgaard et al. (U.S. 5,939,949). Furthermore, in item 7 of the Office action, the Examiner rejected claim 20 as being unpatentable over Hirano et al. in view of Olgaard et al. and Tomassetti et al. (U.S. 5,043,677).

However, in item 8 of the Office action, the Examiner objected to claims 13-17 but indicated that they would be allowable if rewritten as independent claims containing all of the features of their base claim plus any intervening dependent claims. Accordingly, claim 11 has been canceled and claim 13 has been rewritten as an independent claim. The dependency of the remaining claims has been amended to depend ultimately on claim 13. Therefore, the rejections are now moot.

In view of the foregoing, reconsideration and allowance of claims 12-27 are solicited. In the event the Examiner should still find any of the claims to be unpatentable, please telephone counsel so that patentable language can be substituted.

If an extension of time for this paper is required, petition for extension of time is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

LOREN DONALD PEARSON
REG. NO. 42,987

For Applicants

LDP:cgm

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Version with Markings to Show Changes Made:

In the Claims:

Cancel claim 11.

Claim 12 (amended). The current source circuit according to claim [11] 13, wherein said first driver stage forms a part of a current mirror circuit receiving a flow of a stabilized current when said first driver stage is switched on.

Claim 13 (amended). [The] A controllable current source circuit [according to claim 11, wherein] , comprising:

an output;

a supply voltage terminal and a reference potential terminal;

a first driver stage having a first controlled path containing a first transistor and a second driver stage having a second controlled path containing a second transistor, said first and second controlled paths connected in series between said voltage supply terminal and said reference potential terminal, and said second driver stage [forms] forming a part of a current mirror circuit causing a constant stabilized current to flow in said second driver stage; and

only said first driver stage switching on and off in dependence on an input signal, and said second driver stage being switched on and carrying a stabilized current.

Claim 14 (amended). The current source circuit according to claim 13, wherein said current mirror circuit is coupled to a current mirror circuit connected to said first driver stage and causes a [stabilized] current to flow in said current mirror circuit connected to said first driver stage.

Claim 18 (amended). A phase locked loop, comprising:

a phase comparator having a phase comparison circuit with a reference signal input for receiving a reference signal and an input for receiving an input signal whose phase angle is to be regulated, and having a controllable current source circuit according to claim [1] 13 on an output side of said phase comparator;

a loop filter connected to said current source circuit and having an output for outputting an output signal controlling the phase angle of the input signal.

Add the following claims:

~~22~~ 7. The phase locked loop according to claim ~~18~~, wherein said first driver stage of said controllable current source

circuit forms a part of a current mirror circuit receiving a flow of a stabilized current when said first driver stage is switched on.--

--12. The phase locked loop according to claim 7, wherein said current mirror circuit of said controllable current source circuit is coupled to a current mirror circuit connected to said first driver stage and causes a stabilized current to flow in said current mirror circuit connected to said first driver stage.--

--13. The phase locked loop according to claim 7, wherein a current carried by said first driver stage of said controllable current source circuit when said first driver stage is switched on is greater than a current carried by said second driver stage.--

--14. The phase locked loop according to claim 13, wherein the current carried in said first driver stage of said controllable current source circuit is multiple times greater than the current carried by said second driver stage.--

--15. The phase locked loop according to claim 13, wherein the current carried in said first driver stage of said controllable current source circuit is four times greater than the current carried by said second driver stage.--

16 --~~27~~. The current source circuit according to claim ~~14~~, 3 wherein said second driver stage includes:

a circuit node;

a control electrode;

a first and a second current path connected between said supply voltage terminal and said circuit node;

one of said first and said second current paths forming a part of said current mirror circuit connected to said first driver stage; and

a transistor connected between said circuit node and said reference potential terminal, said transistor having a transistor control electrode connected to said control electrode of said second driver stage.--